

**USER’S**

**MANUAL**

*Test Suite*

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**Revision Sheet**

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**1.0 GENERAL INFORMATION**

# GENERAL INFORMATION

## 1.1 System Overview

### 1.1.1 Test Bench

Test Bench is a domain specific part of the toolchain for our framework. In the scope of this study, Test Bench is based on FPGA environment. In this domain, Test Benches are pieces of Verilog codes that are used during FPGA or ASIC simulations. Simulation is a critical step when designing a new hardware system. We need to be sure that our FPGA or ASIC design covers system requirements. Furthermore, test benches are used to simulate the designs without the need of any physical hardware. Therefore, it is easy to test all system functions without real hardware.

The test bench provides some parameters to test functionality of the FPGA device. The DUT calculates some values of these parameters and let the test bench to compare it with the actual outputs.

After the optimal test sequences are generated, these cases must be applied to the target system. In our study, this target system is an FPGA-based system (traffic light control system). We designed a test bench using Verilog Language for this purpose.

### 1.1.2 Test Suite Analyzer

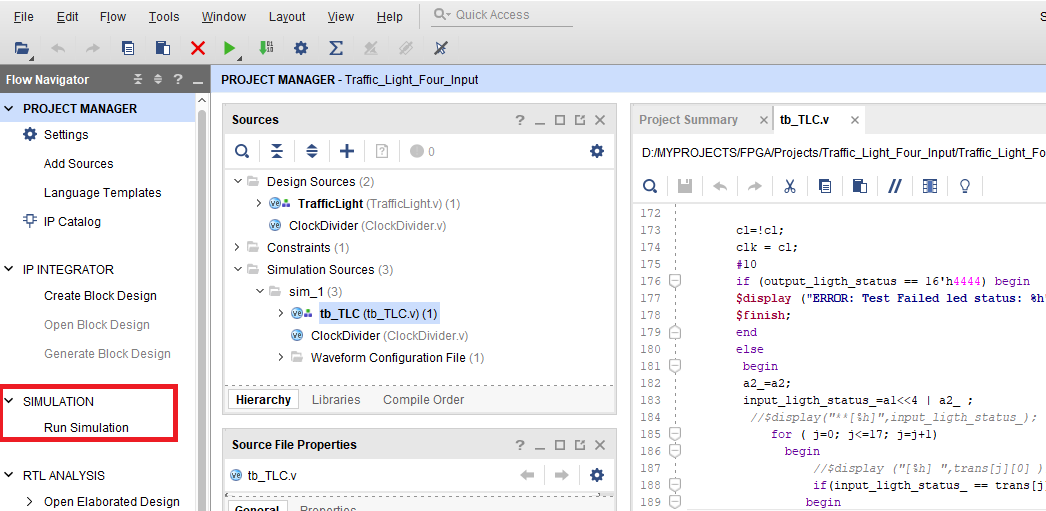
Test suite analyzer analyzes the results collected from the Test Bench to verify the requirements of ideal testing. As already defined in approach section, there are four requirements to fulfill. Test suite analyzer tool collects the test sequences that comply with these requirements to achieve ideal test suite at the end for fault-free and faulty (mutant) designs.

**2.0 SYSTEM SUMMARY**

# TEST BENCH and TEST SUITE ANALYZER

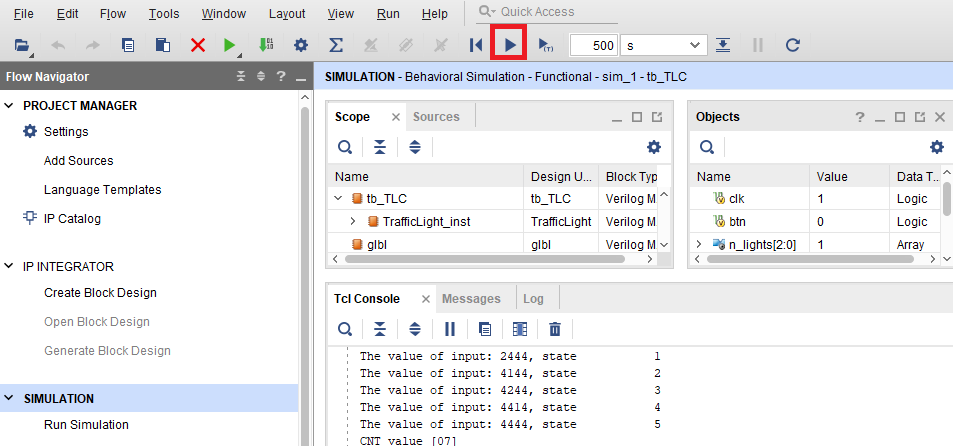
## 2.1 Test Bench

In Vivado IDE click the “Run Simulation” Button.

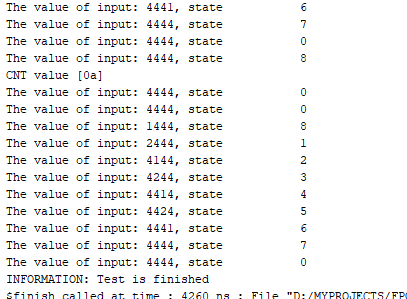


Figure

After that click the play button. (Figure 2)



Figure



Figure